occur at the p-n junction of the contact layer **6***b* and the n-type pillar layer **3** but not at the Schottky junction **11**. This is also effective for achieving the large avalanche withstand capability.

Third Embodiment

[0051] FIG. **7** is a cross-sectional view of main components of a semiconductor device according to a third embodiment of the invention.

[0052] In the structure shown in FIG. **7**, the base layer **5** is formed deeper than the trench gate and covers part of the gate bottom. This reduces a substantial facing area of the control electrode **9** and the first main electrode (drain electrode) **1**, lowers capacitance between the gate and the drain, and then high speed switching becomes possible.

[0053] Moreover, the base layer **5** is formed deeply, and thus the avalanche breakdown is easy to occur at the bottom of the base layer **5** but not at the bottom of the trench gate. Therefore, the hole generated by the avalanche breakdown is drained rapidly from the base layer **5** to the second main electrode (source electrode) **10** through the p^+-type contact layer **6**, and thus the large avalanche withstand capability can be achieved.

[0054] In the structure shown in FIG. **7**, furthermore as shown in FIG. **8**, the p^+-type contact layer **6***a* is provided on the surface of the n-type pillar layer **3**, and thus even if the hole generated by the avalanche breakdown flows into the Schottky junction **11** side, the hole becomes possible to be drained rapidly through the contact layer **6***a,* and larger avalanche withstand capability can be achieved.

Fourth Embodiment

[0055] FIG. **9** is a cross-sectional view of main components of a semiconductor device according to a fourth embodiment of the invention.

[0056] In the structure shown in FIG. **9**, the MOS gate structure has a planar gate structure. That is, a gate insulating film **18** is provided on a portion extending from the n-type pillar layer **3** to the source layer **7** through the base layer **5**, and a control electrode (gate electrode) **19** is provided on the gate insulating film **18**,

[0057] The control electrode **19** is located on the boundary (p-n junction) between the p-type pillar layer **4** and the n-type pillar layer **3**, and the Schottky junction **11** made of the second main electrode **10** and the n-type pillar layer **3** is formed on the surface of the n-type pillar layer **3** between adjacent control electrodes **19** located on this p-n junction. Similar to the embodiment described above, this structure allows a structure integrating the MOSFET with a super junction structure and the Schottky barrier diode in a unit cell to be realized while maintaining a low ON resistance. That is, also in this embodiment, it is possible to make one n-type pillar layer **3** in the unit cell operate as a drift layer common to both of the MOSFET and the Schottky barrier diode.

[0058] The planar gate structure reduces the electric field at an end portion of the control electrode **19** in comparison with the trench gate structure and high gate reliability is achieved.

[0059] In the structure shown in FIG. **9**, furthermore as shown in FIG. **10**, the p^+-type contact layer **6***a* is added on the surface of the n-type pillar layer **3**, and thus it is possible to reduce the electric field at the end of the control electrode **19**. Moreover, it becomes possible to drain the hole generated on application of high voltage from the contact layer **6***a* and the large avalanche withstand capability can be achieved.

Fifth Embodiment

[0060] FIG. **11** is a cross-sectional view of main components of a semiconductor device according to a fifth embodiment of the invention.

[0061] In the structure shown in FIG. **11**, the trench structure is not formed at the boundary between the p-type pillar layer **4** and the n-type pillar layer **3**, and the width of the p-type pillar layer **4** is narrower than that of the n-type pillar layer. As for this structure, one n-type pillar layer **3** of the unit cell is shared between the MOSFET and the Schottky barrier diode to form an integrated structure, hence the same effect as the above embodiments is obtained. However, in this structure, the width of the n-type pillar layer **3** is broad, and a resistance for broadening a current path is generated, thereby structures of above respective embodiments have a lower ON resistance.

[0062] As shown in FIG. **12**, the p-type pillar layer **4** is provided not only under the base layer **5** but also in the n-type pillar layer **3** between the trench gates, and a lateral period of the super junction structure is ½ times of a lateral period of the base layer **5**, and thereby the ON resistance can be reduced. That is, narrowing the lateral period of the super junction structure allows an impurity concentration in the p-type pillar layer **4** and the n-type pillar layer **3** to be higher, and thereby the low ON resistance can be achieved.

[0063] As for this structure, one n-type pillar layer **3** of the unit cell is shared between the MOSFET and the Schottky barrier diode to form an integrated structure, hence the same effect as the above embodiments is achieved.

[0064] In the structure in FIG. **12**, furthermore as shown in FIG. **13**, the p^+-type pillar layer **6***b* is formed in the superficial portion of the p-type pillar layer **4** not existing below the base layer **5**, and thereby it becomes possible to drain the hole generated by the avalanche breakdown on application of high voltage through the contact layer **6***b* and the large avalanche withstand capability can be achieved.

[0065] Even if the avalanche breakdown does not occur, the pi-type pillar layer **4** is depleted by application of high voltage. At the time of forward recovery of the Schottky barrier diode to forward bias, hole supply is needed for releasing the depletion of the p-type pillar layer **4**. However, formation of the above contact layer **6***b* reduces a contact resistance between the p-type pillar layer **4** and the second main electrode (source electrode) **10**, and realizes rapid hole supply from the second main electrode **10**. This reduces the ON voltage rapidly at the forward recovery of the Schottky barrier diode, and can realize low recovery loss.

[0066] The embodiment of the invention has been described with reference to the specific examples. However, the invention is not limited thereto, but can be variously modified in accordance with the spirit of the invention.

[0067] For example, in the embodiment describe above, the description has been made under that the first conductivity type is the n-type and the second conductivity type is the p-type, however, the invention can be practiced also under that the first conductivity type is the p-type and the second conductivity type is the n-type.

[0068] The plane pattern of the MOS gate section and the super junction structure may be formed in a lattice, a staggered, or a hexagonal configuration without limit to a striped configuration.